AMENDMENT TO THE SPECIFICATION

Please amend the paragraph at page 12, line 24 to page 13, line 5, as follows:

The system includes two processor engines, representing a migrant engine 400 (that is, a processor implementing a first instruction set architecture) with processing resources, including a register file 402, used for processing instructions from the first instruction set architecture, and a native engine 404 (that is, a processor implementing a second instruction set architecture) with processing resources, including a register file 406, optionally containing tags 408, which may contain, for instance, information about misspeculation and exception recovery for aggressive ILP compilation, and a shadow memory 410, used for storing instructions from ~~form~~ the second instruction set architecture. The shadow memory is not used by and/or is inaccessible to migrant engine 400.